**Lab 5 & 6: Assignment 1 (10 Marks)**

**Date for Showing the output to Instructor (No Deduction): 17/09/2021 between 11AM-1PM**

**Due Date for final submission through CMS: 17/09/2021 9:00 PM**

**Name**: Lakshmi Mounika Chaturvedula

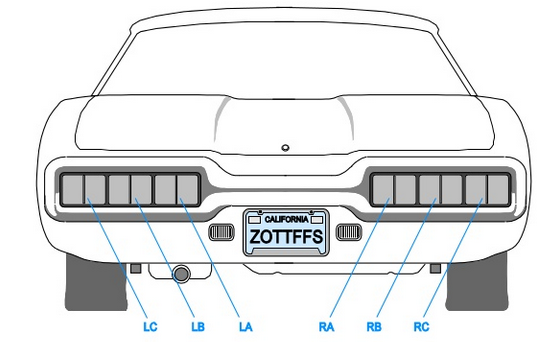
**ID No**: 2019A8PS0621H

**Problem Statement:** Design a state machine to control the tail lights of a 1965 Ford Thunder bird (Figure 1). The tail lights are composed of three lights on each side which operate for the turns as shown in figure 2. The state machine has two inputs **(LEFT, RIGHT)** and 6 outputs **(LC, LB, LA, RA, RB and RC)**. When **(RIGHT=0 and LEFT=0)** or when **(RIGHT=1 and LEFT=1)** no lights will turn ON. If **(RIGHT=0 and LEFT=1)** then lights LC, LB, and LA will be ON as shown in figure 2(a) indicating **LEFT** turn. If **(RIGHT=1 and LEFT=0)** then lights RA, RB, and RC will be ON as shown in figure 2(b) indicating **RIGHT** turn. In addition to LEFT and RIGHT there are two more inputs **Clk** and **Reset** for normal operation of FSM. When **Reset** is enabled all lights will be OFF**.** The flashing rate of LEDs is 2Hz (i.e. the time between two successive states is 0.5s).

**PIN Assignment:**

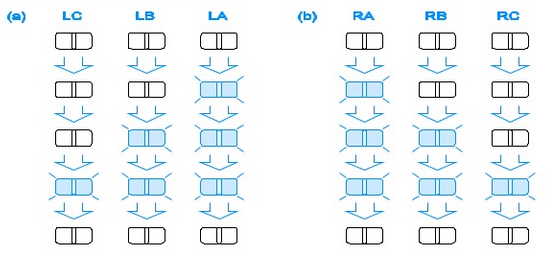
**Inputs: RIGHT🡪 F22; LEFT🡪G22;**

**Outputs: LC🡪U14; LB🡪U19; LA🡪W22; RA🡪U22; RB🡪T21; RC🡪T22;**



**Figure 1**

**Left Turn Right Turn**

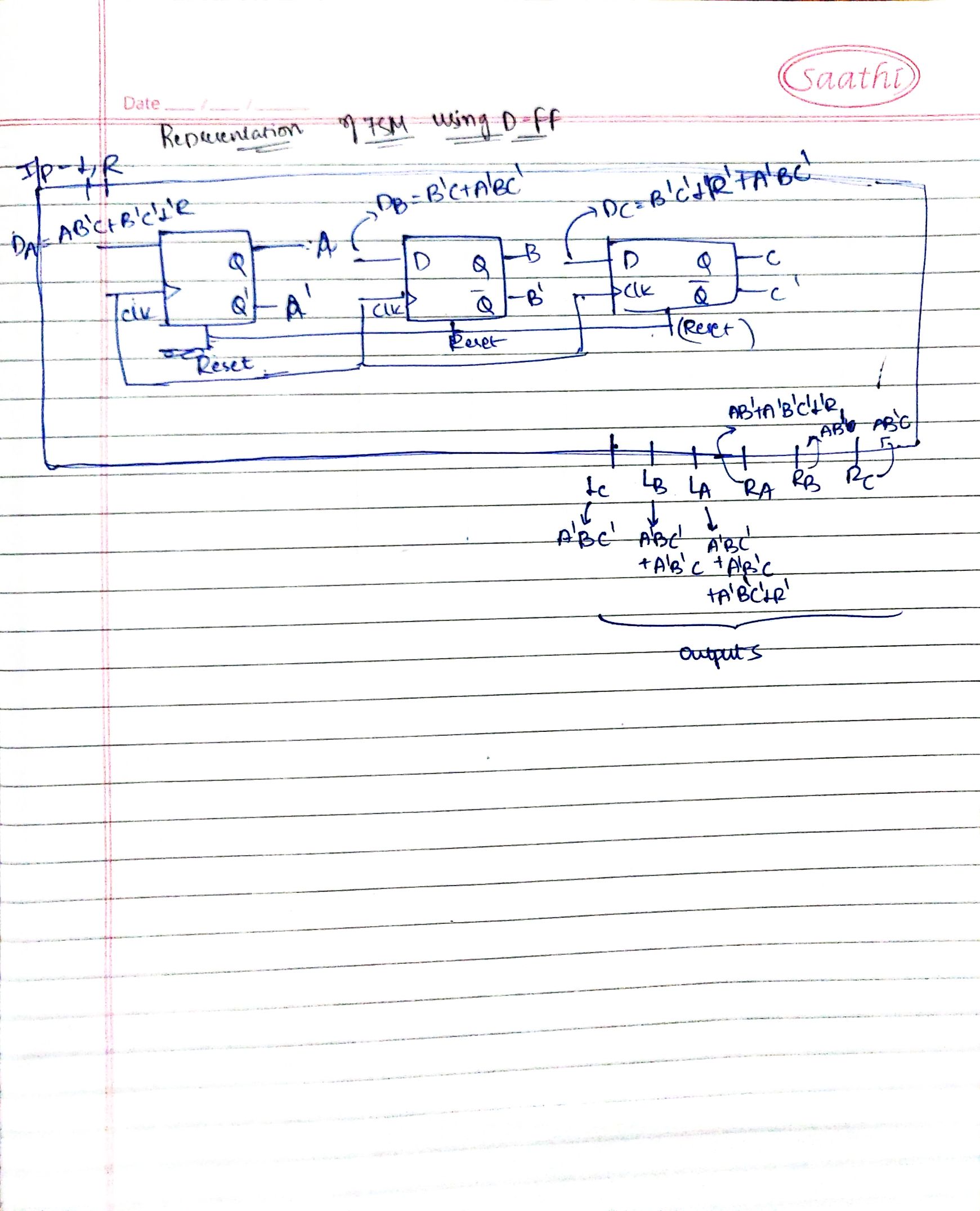
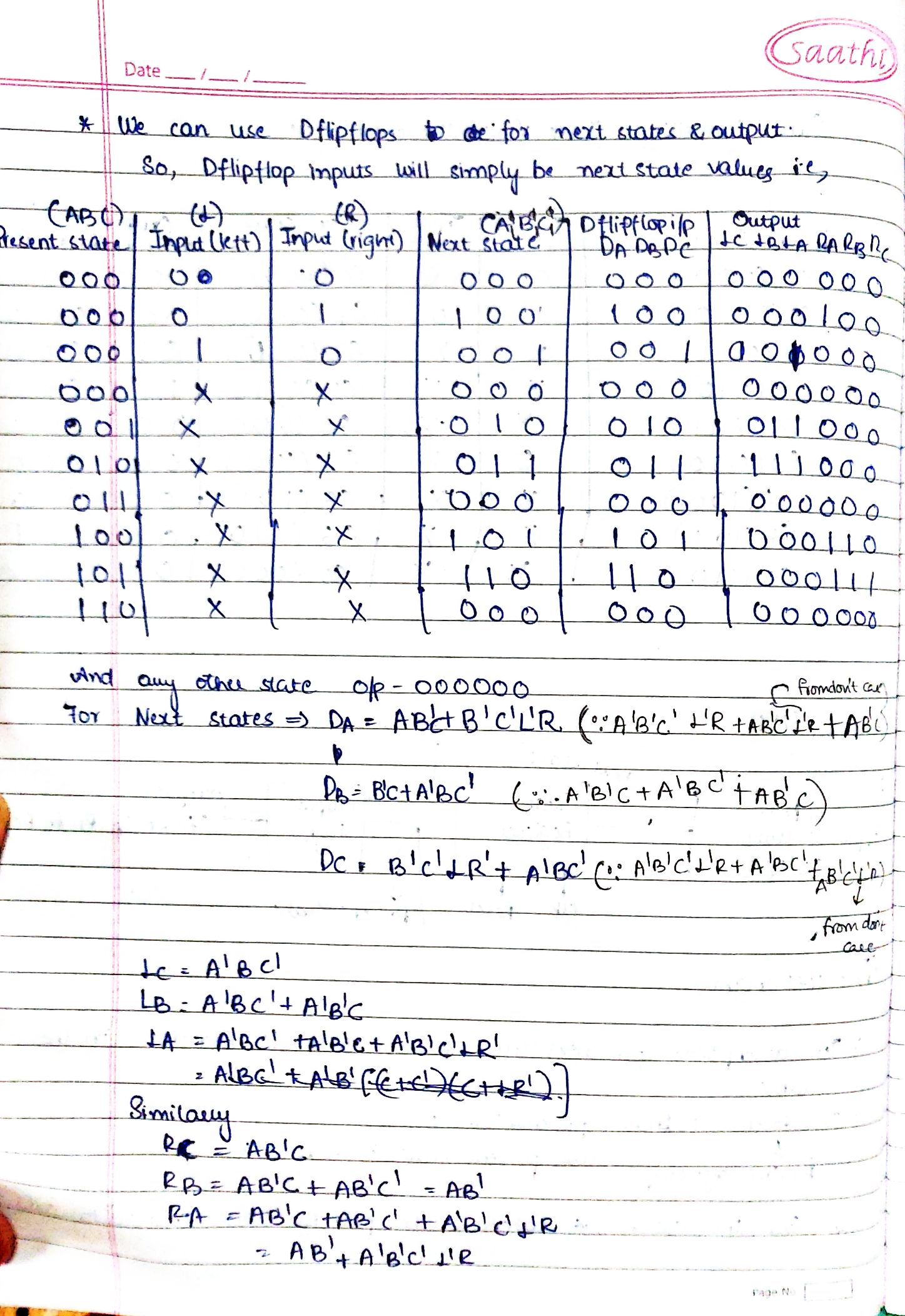
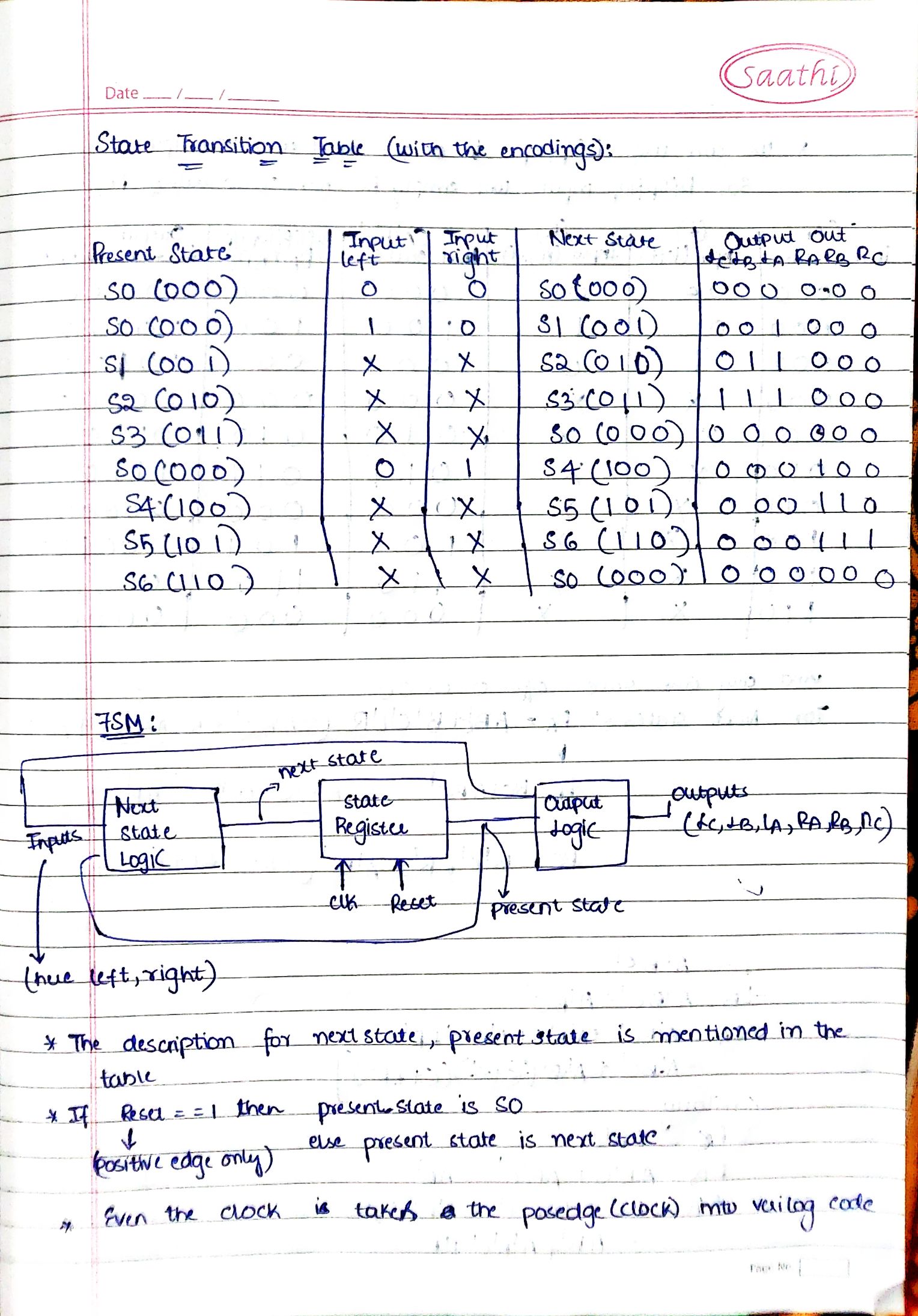
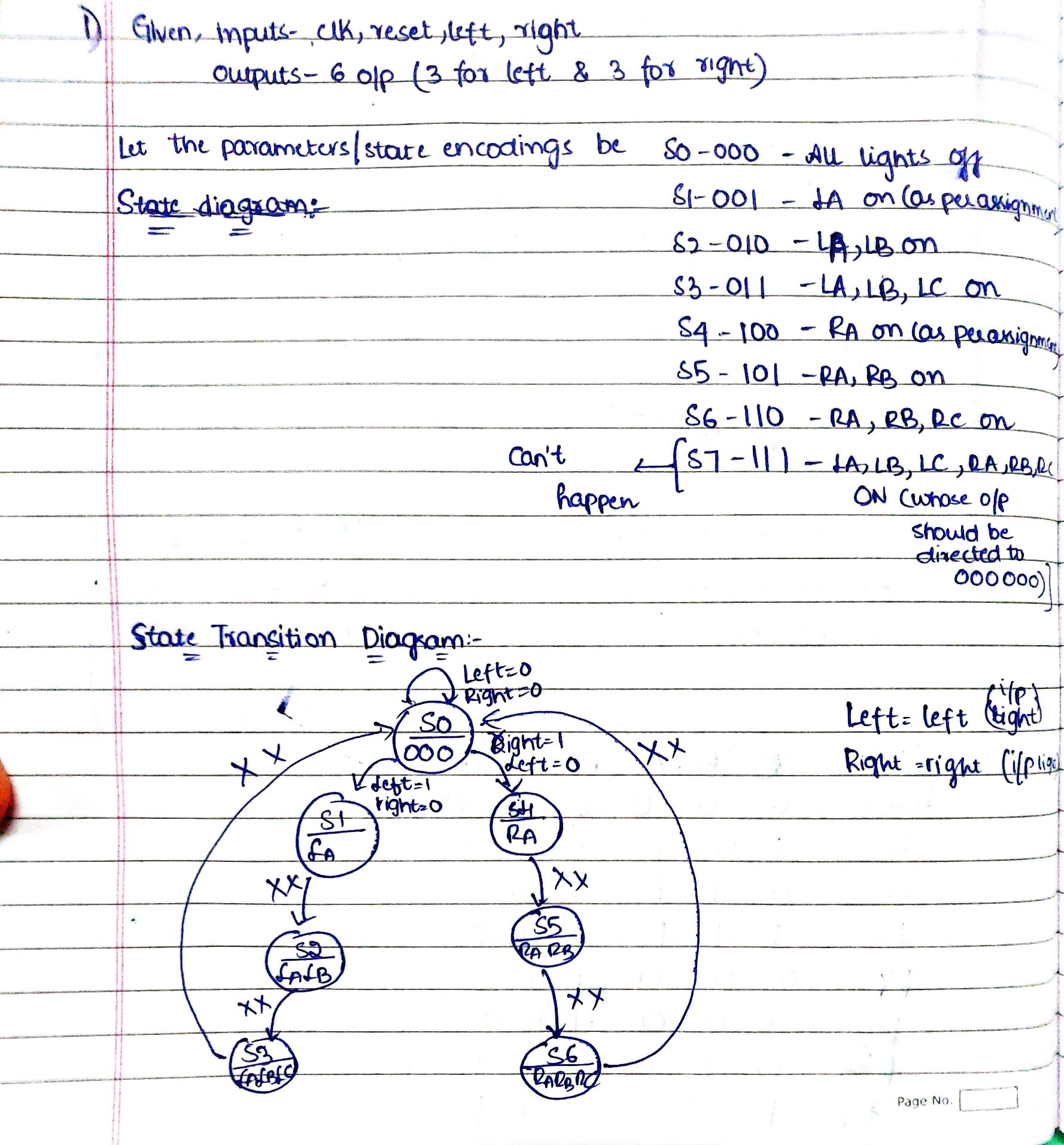


**Figure 2(a) Figure 2(b)**

**Figure 2**

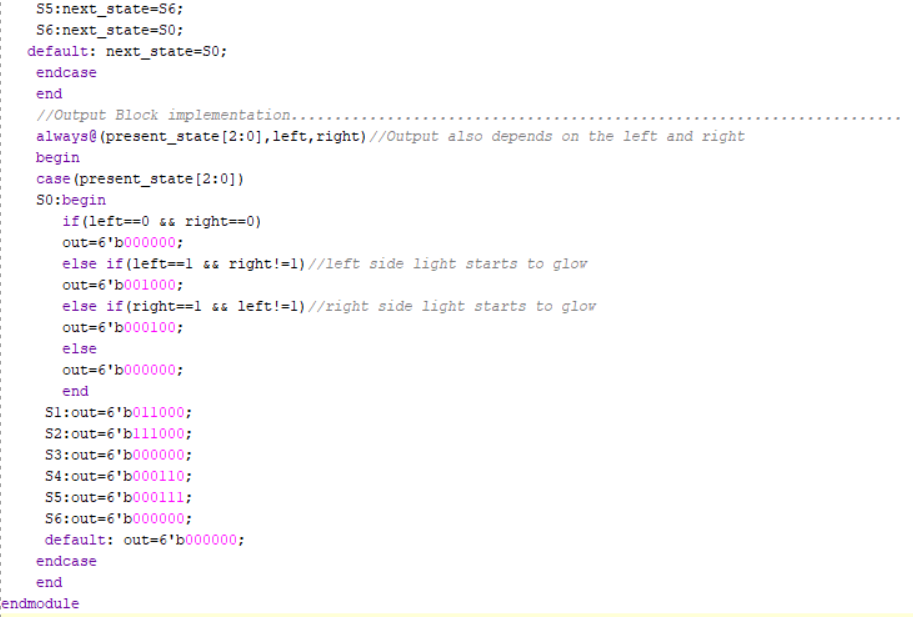
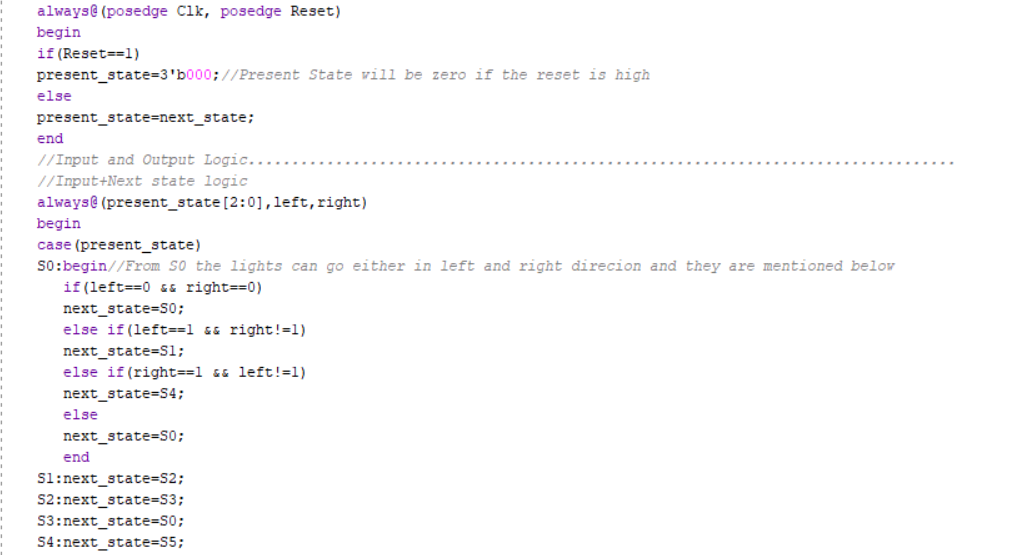
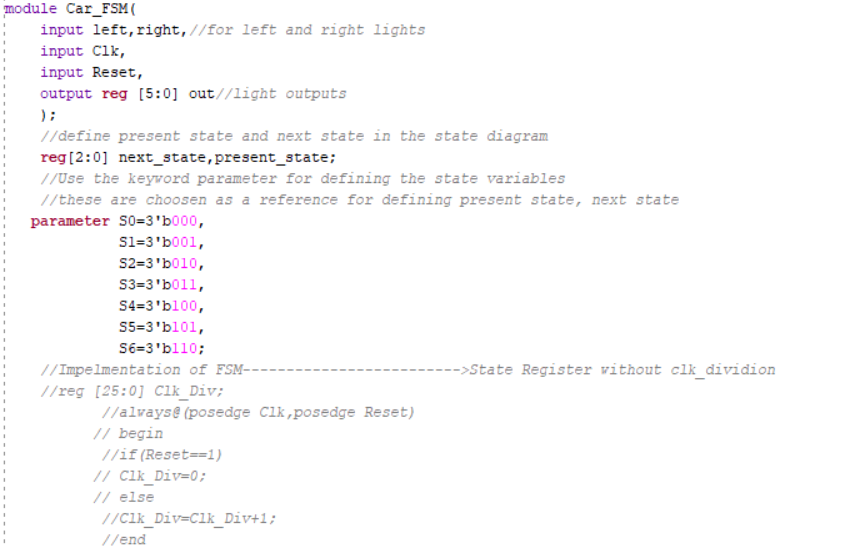
(Please refer to the file named “**Vivado\_Design\_Flow\_All\_Steps.pdf**” for a review of all the steps in the design flow)

1. **Question: Draw the FSM (can be an image) with proper description.**

Answer:

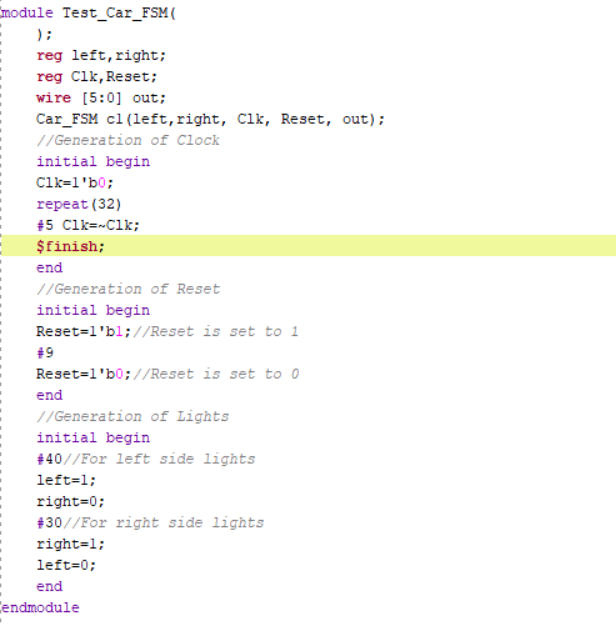
1. Create a Vivado Project and write Verilog code (**Car\_FSM.v** with comments) for implementing the above FSM.

**Question: Paste the image of verilog code Car\_FSM.v.**

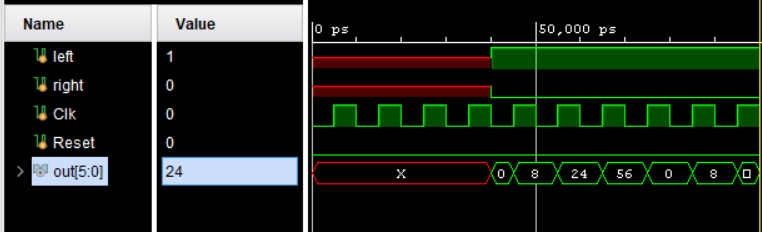
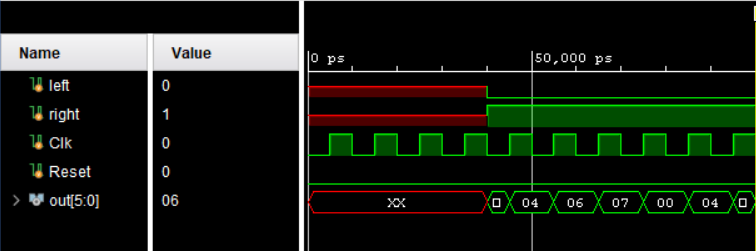
Answer: Without the clock division

1. Write the test bench **Test\_Car\_FSM.v** and simulate your design to check the functionality.

**Question: Paste the image of test bench verilog code Test\_Car\_FSM.v.**

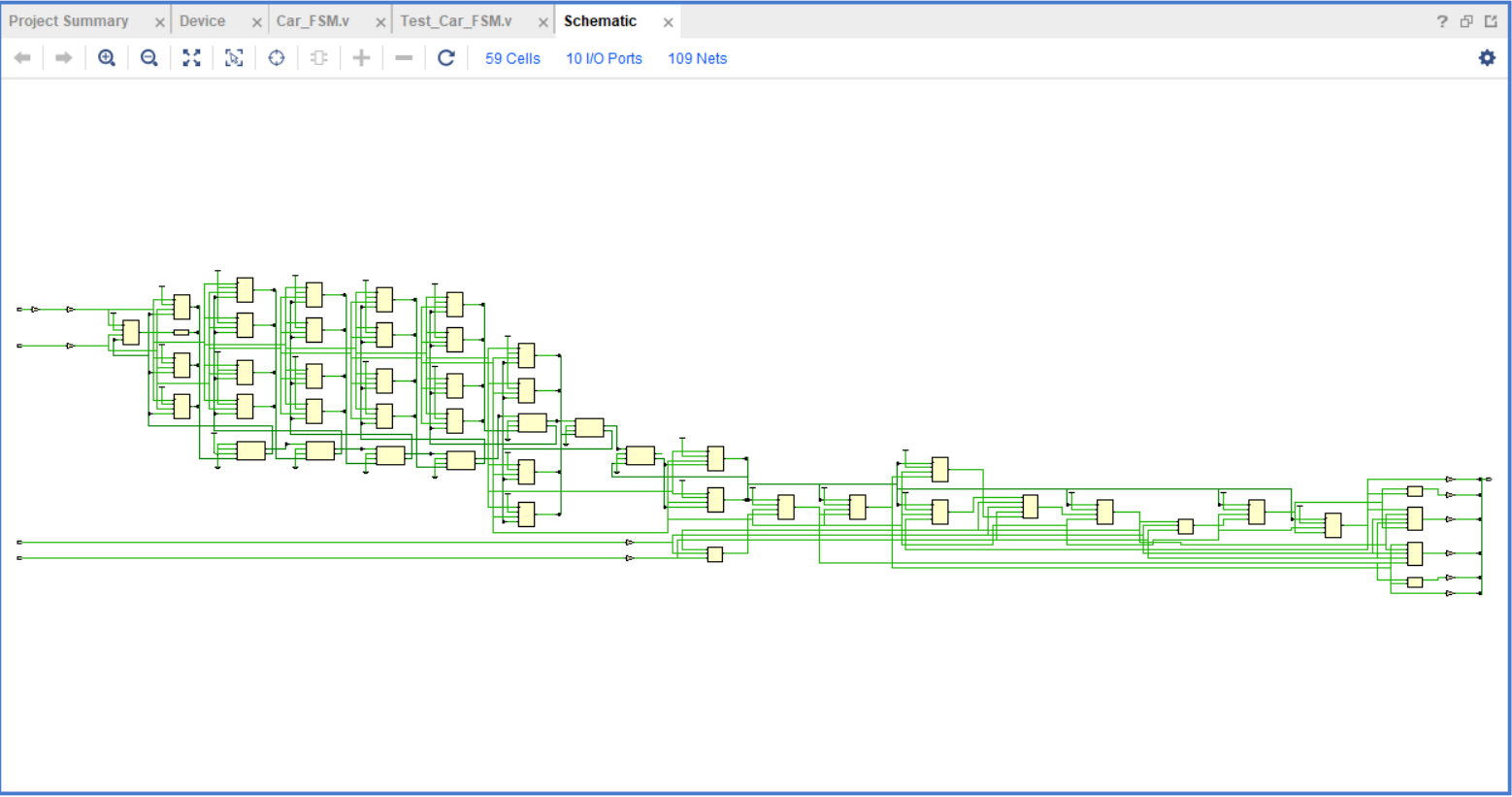
Answer: 

**Question: Paste the image showing the simulated waveforms for FSM (Behavioral Simulation). Clearly show the LEFT turn and RIGHT turn Cases.**

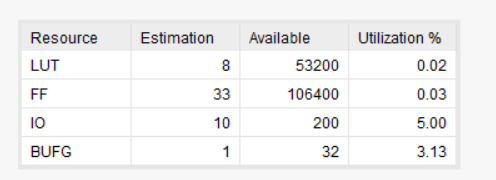
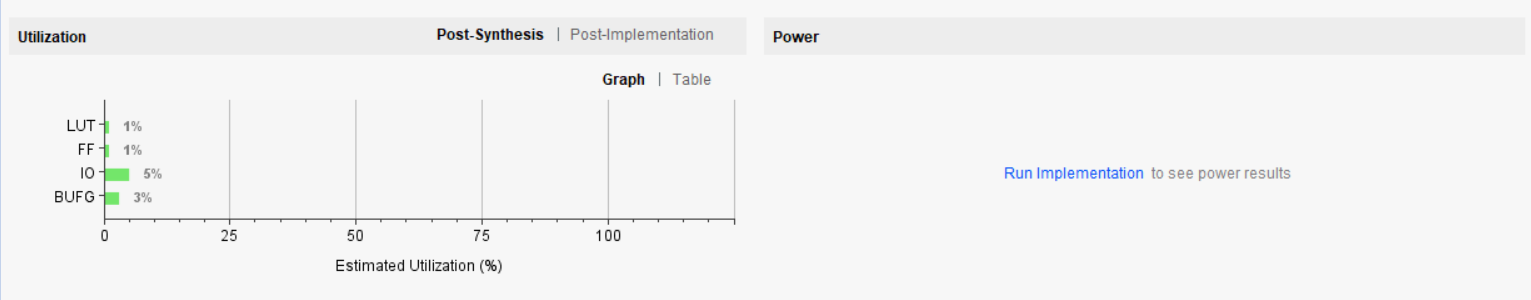
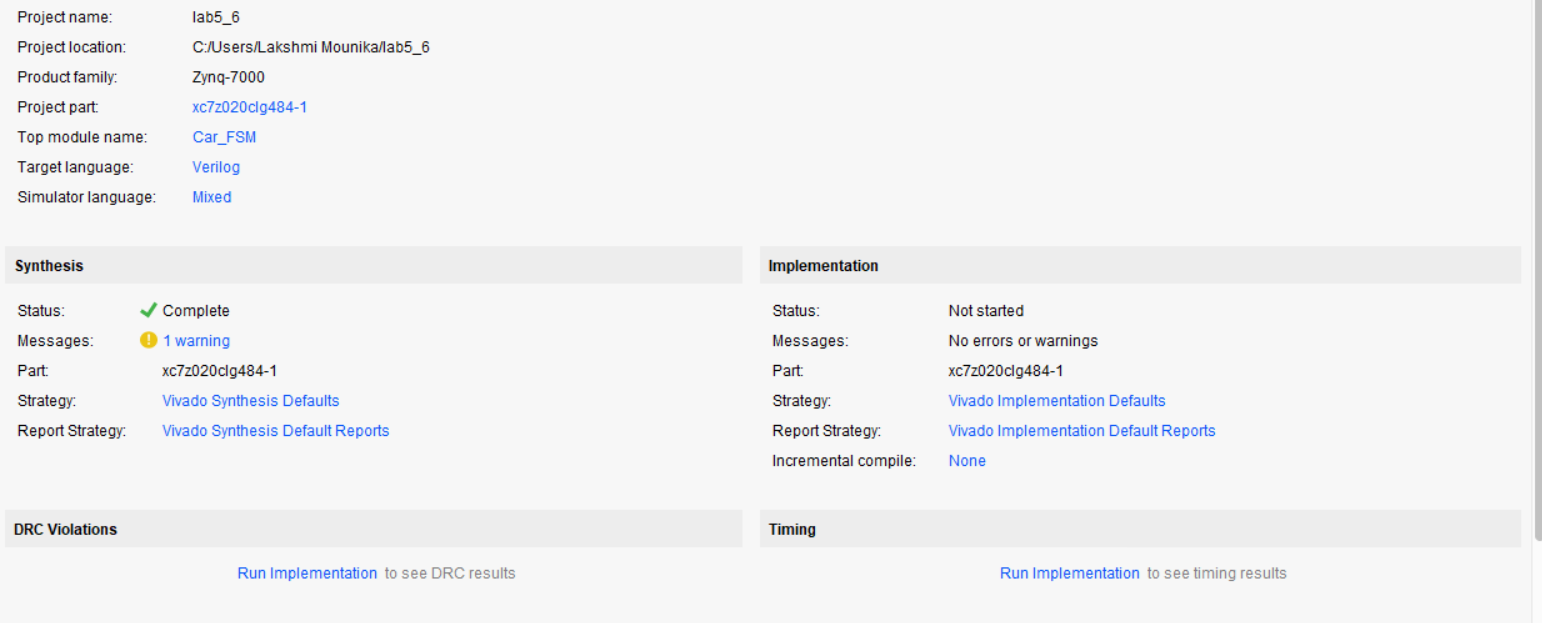
Answer: LEFT TURN: 0001000-8; 011000-24; 111000-56 (Put Left=1 and Right=0 in the Test Bench)RIGHT TURN: 000100-4;000110-6;000111-7 (Put Right= 1 and Left=0 in the Test Bench) 

1. Add clock division code to **Car\_FSM.v** such that the actual input **Clk (Y9 pin with frequency of 100MHz)** is converted to Clock of frequency 2Hz. This 2Hz signal is used as clock for running the FSM.
2. Plan your I/O mapping (using **I/O planning** option) such that actual input **Clk** is connected to internal clock pin **Y9**, **Reset** is connected to push button switch, other inputs (**LEFT** and **RIGHT**) are connected to DIP switches and outputs are connected to LEDs. In the ZedBoard, the pin numbers indicating the DIP switches, LEDs and internal clock are listed in table uploaded in CMS. Save the mapping information as **Car\_FSM.xdc**.
3. Synthesize (**Run Synthesis**).

**Question: Paste the image showing the schematic after synthesis.**

Answer: 

**Question: Check the summary report and report hardware utilization for the FSM implementation.**

Answer: Hardware Utilization=5+3.13+0.03+0.02=8.18%

1. Implement the design (**Run Implementation)**.
2. **Generate Bitstream** and port your design on to FPGA (**Open Hardware Manager**🡪 **New Target**🡪… **Program Device**)
3. **Check the output on FPGA.**
4. **Show the output to the instructor.**
5. **Submit following files as a Zipped folder with file name as <Student1\_ID\_No>\_<Name>.zip through CMS before due date.**

**1) Completed Document**

**2) Car\_FSM.v (with proper comments)**

**3) Test\_Car\_FSM.v (with proper comments)**

**4)** **Car\_FSM.xdc**.

**5) Car\_FSM**.**bit**